REMARKS

Claims 1-51 are pending in the application and stand rejected. Claims 43, 44, 47 and 48 have been amended. Applicants respectfully request reconsideration of the rejections based on the above amendments and following remarks.

Claim Rejections - 35 U.S.C. § 101

Claims 1-3, 5, 8-11, 14, 42 and 36 stand rejected as being directed to non-statutory subject matter for the reasons set forth on page 2 of the Office Action. Applicants traverse the rejection. Examiner contends, without explanation, that the claimed inventions are directed to an abstract idea. However, claim 1 is directed to an automated method for managing a plurality of cachable entities. This method is performed by analyzing program code to determine if there is at least one statement which can affect a desirability of performing at least one cache transaction, if the at least one statement is executed. A probability that the at least one statement will execute is then determined, and the desirability of performing the at least one cache transaction is determined based on said probability.

Claim 1 does not amount to some "machine manipulated abstract idea" as baldly stated in the Office Action. Indeed, claim 1 is directed to a patentable cache management method for determining when cache transactions should be performed, which is clearly directed to statutory and patentable subject matter.

If Examiner maintains this rejection, Applicants request that the Examiner provide a reasonably detailed explanation regarding the basis for rejection, which addresses the specific claim language and explains how the specific claimed subject matter amounts to an "abstract idea." Currently, the Office Action's conclusory assertions fail to establish a *prima facie* case of

non-statutory subject matter under 35 U.S.C. 101. Without more, the rejection should be withdrawn.

Double Patenting

Applicants may file a terminal disclaimer, if needed, in due course depending on the scope of allowed claims. At this time, Applicants request that the double patenting rejection be held in abeyance pending the disposition of this application.

Claim Rejections - 35 U.S.C. § 112

(i) Claims 42-44 and 46-51 stand rejected under 35 § U.S.C., first paragraph, for supposedly failing to comply with the written description requirement. Applicants traverse the rejection. At the outset, the Examiner should be reminded that in assessing whether a specification satisfies the "written description" requirement, the fundamental factual inquiry is whether the patent specification describes the claimed invention with *reasonable* clarity such that one of ordinary skill in the art can reasonably conclude that the inventor had possession of the claimed invention as of the filing date of the specification. An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, etc., that fully set forth the claimed invention. However, compliance with the written description requirement does not compel use of any particular form of description, so long as the description clearly allows one of ordinary skill in the art to recognize that the applicant invented what is defined by the patent claims.

Here, at the very least, the specification as originally filed contains sufficient disclosure, either expressly or inherently, to support the claimed inventions 42-44 and 46-51 under the "written description" requirement of 35 U.S.C. 112, first paragraph. Examiner's rejections are

erroneoulsy based on citation to specific portions of Applicants's specification and misplaced reliance on specific terms. However, this is not a proper analysis.

For instance, with respect to claims 42 and 46, claim 1 recites "determining a probability that the at least one statement will execute" and claim 42 recites "determining the probability based on a likelihood of a value of a cachable entity changing (this is similar for claims 18 and 46). The Examiner points to page 36, lines 14-23 of Applicants' specification as being contradictory to the claimed subject matter, but this is rather bewildering because the cited section actually supports the claim language. Moreover, Examiner should review page 36, lines 9-14, for example, which further supports the claimed subject matter.

Further, with respect to claim 43, 44, 47, and 48, Examiner should review page 36, lines 9-23, for example.

With respect to claims 44 and 48, Examiner's should note that the phrase "not exceeding a threshold" is analogous to the phrase "meeting or falling below the threshold". Again, Examiner's written description rejection is this regard is legally erroneous as it is based purely on matching specific claim terms to specification terms, which is not proper.

Finally, with respect to claims 49-51, Examiner's contention that "there is nothing in the specification to indicate that that desirability is a quantified measure" is baseless and misplaced. Examiner should review, for instance, page 38, lines 1-22.

Accordingly, withdrawal of the written description rejections is requested.

(ii) Claim 43, 44, 47 and 48 stand rejected under 35 U.S.C. § 112, second paragraph, for lack of antecedent basis. These claims have been amended to provide antecedent basis for the

term threshold. Accordingly, Accordingly, withdrawal of all rejections under 35 U.S.C. § 112, second paragraph, is requested.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 5, 10, 18, 22, 27, 35, 39, 40, 41 and 45 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 5,940,857 to Nakanishi. Applicants respectfully traverse the rejection. At the very least, Nakanishi. does not disclose or suggest *analyzing program code to determine if there is at least one statement which can affect a desirability of performing at least one cache transaction, if the at least one statement is executed,* as essentially recited in claims 1, 18 and 35.

The Examiner's reliance on Abstract, col. 4, lines 22-44 of Nakanishi in this regard is wholly misplaced. Nakanishi discloses a process of analyzing instructions that are read from a main memory (and being transferred to an instruction cache) to predict whether it is necessary to read out a next block from the main memory. Nakanishi does not disclose or even remotely suggest that the block of instructions read out from main memory are analyzed to determine a statement that if executed, would affect a desirability of performing a cache transaction. It appears that Examiner's reliance on Nakanishi's "instruction analyzing" step is improper and out of context, as such analysis process is dissimilar in function and purpose as the claimed invention. As such, the Examiner should withdraw the anticipation rejections based on Nakanishi.

Claims 1-8, 10, 14-25, 27 and 31-48 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Cytron. For previous reasons submitted by Applicant, claims 1, 18 and 35 are

clearly patentable and non-obvious over Cytron, in that Cytron does not disclose or suggest *analyzing program code to determine if there is at least one statement which can affect a desirability of performing at least one cache transaction, if the at least one statement is executed; determining a probability that the at least one statement will execute; determining the desirability of performing the at least one cache transaction based on the probability that the at least one statement will execute*, as essentially claimed.

Cytron is directed to a compiler-directed cache coherence method for maintaining *cache coherence* in a multiprocessor system wherein each processor has a cache associated therewith and wherein the processors read contents of a shared memory location. In other words, Cytron is concerned with maintaining consistency of cached values in the various caches, which are read by an application. Although Cytron arguably discloses analyzing program code, there is nothing in Cytron that discloses analyzing the code to determine if there is a statement that can affect a desirability of performing a cache transaction, *if the statement is executed*, and then *determining a probability that the statement will execute* and determining the desirability of performing a cache transaction *based on a probability that the statement will execute*.

Moreover, pages 231 and 232, section 2.2, of Cytron (as relied on by Examiner) does not disclose the claimed process of "determining a desirability" is misplaced. In contrast, the cited section 2.2 discloses a method of posting values to a global memory for the purpose of preventing state values from being referenced from the global memory. This has *no* relation whatsoever to *determining the desirability of performing a cache transaction based on a probability that a statement will execute*, as claimed. Indeed, in the "posting" method (equation (1)) there is no need to "determine desirability" of performing a cache transaction because is presumed that the

statement will always execute to update the global memory.

Thus, for at least all of the above reasons, claims 1, 18 and 35 are patentably distinct and patentable over Cytron. In addition, dependent claims 2-8, 10, 14-17, 19-25, 27, 31-34 and 36-48 are patentably distinct and patentable over Cytron at least for the reasons given above for their respective base claims.

Claims 1, 2, 4-6, 8, 18, 19, 21, 23, 25, 35, 36, 38-41 and 45 stand rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,774,685 to Dubey. Again, for reasons previously submitted, the Examiner's reliance on Dubey is wholly misplaced, and clearly does not anticipate the claimed inventions. Dubey is related to a method for performing a compile-time analysis of a program, in which an instruction "STOUCH" enables prefetching data and storing the prefetched data in a cache based on compile-time speculations associated with conditional branches. In short, Dubey discloses a scheme to prefetch data or instructions and place them into a cache to prevent penalties associated with cache misses during program execution.

Examiner relies on Dubey at Col. 3, line 58- Col. 4, line 4 as disclosing the claimed "analyzing" process, but such reliance is respectfully misplaced. Dubey discloses in the cited section a "prefetching scheme base on compile-time analysis to determine specification locations within a program where instructions or data cache misses are likely to be encountered at run-time". In other words, Dubey discloses analyzing program code to identify "prefetch points" or points at which data or instructions can be prefetched from main memory, for instance (see, Col. 3, lines 27-38). When the teachings of Dubey and the claimed inventions are construed in proper context, and not in a vacuum, it is clear that Dubey does not disclose analyzing program code to

make determinations as to the "desirability" of performing a cache transaction, as contemplated by the claimed inventions.

Accordingly, claims 1, 18 and 35 (and all claims that depend there from) are patentable over Dubey. Therefore, withdrawal of the anticipation rejections is requested.

Claim Rejections - 35 U.S.C. § 103

Claims 9 and 26 stand rejected as being unpatentable over Cytron in view of U.S. Patent No. 6,073,129 to Levine, et al. The rejection of claim 9 and 26 is based, in part, on the contention that Cytron discloses the elements of claims 1 and 18 from which claims 9 and 26 respectively depend. However, at the very least, the obviousness rejection is invalid by virtue of Cytron failing to disclose or suggest all elements of base claims 1 and 18. Further, it is unquestionable that Levine fails to cure the deficiencies of Cytron with respect to claims 1 and 18 as discussed above. Accordingly, withdrawal of the obviousness rejections is requested.

Early and favorable consideration of this application is respectfully requested.

Respectfully submitted,

Frank V. DeRosa
Reg. No. 43,584
Attorney for Applicant(s)

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, New York 11797
TEL.: (516) 692-8888
FAX: (516) 692-8889